OUM - A 180 nm Nonvolatile Memory Cell Element Technology For Stand Alone and Embedded Applications

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ABSTRACT

This paper discusses the development status of the memory cell element of OUM (Ovonic Unified Memory) - a chalcogenide-based, phase-change nonvolatile semiconductor memory technology at the 180 nm technology node. The device structure and characterization of the memory element will be reviewed. The key characteristics of the technology will be discussed for ultra-high density, low voltage, high-speed programming, high cycle count, high read speed, and competitive cost structure nonvolatile memory for stand alone and embedded applications. This technology is inherently radiation resistant and is bit, byte or word programmable without the requirement of Flash-like block erase. Low voltage and energy operation make OUM an attractive candidate for mobile applications.

INTRODUCTION

There is a growing need for a nonvolatile memory technology for high density stand alone and embedded CMOS applications with faster write speed and higher endurance than existing nonvolatile memories. OUM is a promising technology to meet this need. A phase-change memory array based on chalcogenide materials originally was reported by R.G. Neale, D.L. Nelson and Gordon E. Moore in 1970 (1). Improvements in phase-change materials technology subsequently paved the way for development of commercially available rewriteable CD and DVD optical memory disks (2). These advances, coupled with significant technology scaling and better understanding of the fundamental electrical device operation, have motivated development of the OUM technology at the present day technology node (3,4).

OUM is a nonvolatile memory that utilizes a reversible structural phase change between amorphous and polycrystalline states in a GeSbTe chalcogenide alloy material. This transition is accomplished by heating a small volume of the material with a write current pulse and results in a considerable change in alloy resistivity. The amorphous phase has high resistance and is defined as the RESET state. The low resistance polycrystalline phase is defined as the SET state.

A comparison of OUM with other nonvolatile memories as well as with volatile DRAM and SRAM memory is shown in Table 1. Distinct competitive advantages for a technology are indicated in the table with shaded boxes. Key advantages of OUM nonvolatile technology are: write/read performance, endurance, scalability, low programming energy, process simplicity, cost, and CMOS embeddability. The write/read performance is comparable to DRAM. The OUM technology offers overwrite capability, and bit/byte data can be written randomly with no block erase required. Write endurance is competitive with other potential nonvolatile memory technologies, is superior to Flash and is adequate for many DRAM/SRAM applications. Read endurance is unlimited. Scaling is a key potential advantage of OUM. Write speed and write energy both scale with programmed media volume. Its low voltage operation is compatible with continued CMOS feature and power supply scaling. Due to the ultra-small volume of actual media programmed, the OUM cell size scaling is limited predominantly by column and row pitch lithography. Low voltage operation and short programming pulse widths

TABLE 1 - Memory Technologies Comparison

	DRAM	SRAM (6T)	FLASH	OUM	MTJ-RAM	FERAM
Cell size (F^2)	6 - 12	50-80	7 - 11	5-8	???	Large
Volume @ .18uM (F^3)	17	80	1	0.028	???	Large
Volatile / Non-volatile	Volatile	Volatile	Non-volatile	Non-volatile	Non-volatile	Non-volatile
Endurance write/read	∞ / ∞	∞ / ∞	1E6 / ∞	>1E12 / ∞	> 1E12 / ∞	1E12 / 1E12
Read	Destructive	Partial-destructive	Non-destructive	Non-destructive	Non-destructive	Destructive
Direct Over-write	Yes	Yes	No	Yes	Yes	Yes
Bit/Byte Write/Erase	Yes	Yes	Block	Yes	Yes	Yes
Read dynamic range (margin)	100-200mV	100-200mV	Delta Current	10X - 100X R	20-40% R	100-200mV
Programming energy	Medium	Medium	High	Low	Medium	Medium
Write / Erase / Read time	50nS / 50ns / 50ns	8ns / 8 ns/ 8 ns	1uS / 1-100ms(block)/ 60 ns	10ns / 50ns / 20ns	30nS / 30ns / 30ns	80ns / 80ns / 80ns
Transistors	Low performance	High performance	High voltage	High performance	High performance	Low performance
CMOS Logic Compatibility	Bad	Good	OK, but Hi V req'd	Good	???	OK, but Hi V req'd
New Materials	Yes	No	No	Yes	Yes	Yes
Scalability Limits	Capacitor	6T	Tunnel Oxide /HV	Litho	Current Density	Polarizable Capacitor
Multi-bit storage	No	No	Yes	Yes	No	No
3D Potential	No	No	No	Yes	???	???
SER Susceptibility	Yes	Yes	No	No	No	Yes
Relative Cost per Bit	Low	High	Medium	Low	???	High

yield low energy operation for the OUM, a key metric for mobile portable applications.

The OUM device is a thin-film, low topology two-terminal device providing process simplicity using conventional processing tools and unit process steps. Competitive cell size and relative process simplicity provide the potential for low cost per bit. The large resistance distinction between states allows for ample read margin. Multi-bit per cell storage capability is possible with OUM because of the wide operating range of programmed resistance. Since memory media is integrated after transistor formation and prior to metallization, embedding into a state-of-the-art baseline CMOS logic or logic/analog process is relatively easily achieved.

TECHNOLOGY AND DEVICE PERFORMANCE

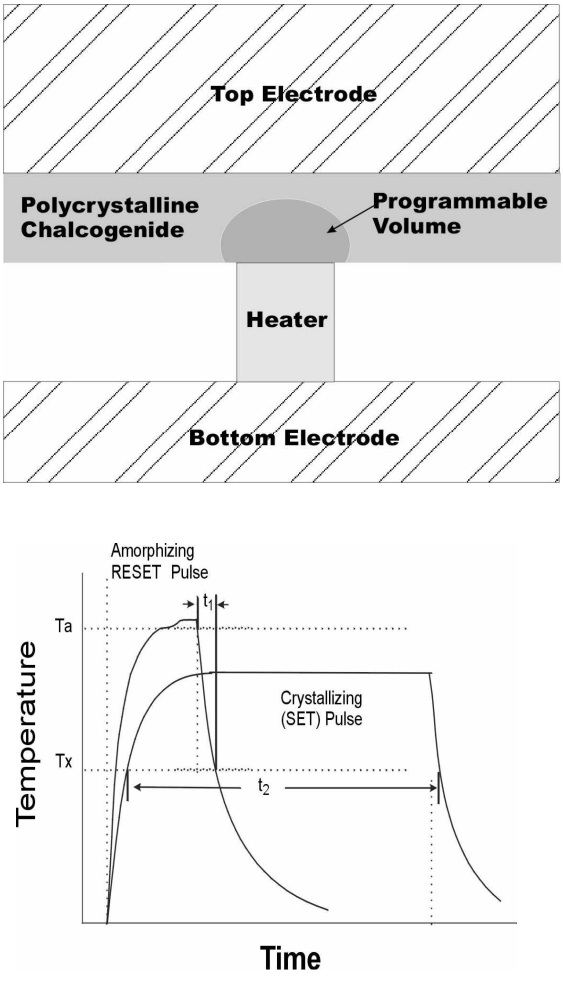

Fig. 1 (a) Schematic cross-section of the memory element (b) depiction of the time (pulse width) - temperature relationship of the phase change process.

Temperature steps required to form the OUM elements do not compromise transistor performance, and the OUM elements are able to withstand subsequent multi-level film depositions and their associated temperatures and gas ambients.

Fig. 1 shows a schematic illustration of the cross section of an OUM memory cell element. Because of the very small size of the OUM, the thermal time constant of the device is short -- on the order of a nanosecond. During the amorphizing reset pulse, the temperature of the programmed volume of phase-change material exceeds the melting point which eliminates the polycrystalline order in the material. When the reset pulse is terminated, the device quenches to "freeze in" the disordered structural state. This quench time (t1~1ns) is determined by the thermal environment of the device and the fall time of the pulse. The crystallizing set pulse is of lower amplitude and of sufficient duration (t2~50ns) to maintain device temperature in the rapid crystallization range for a time sufficient for crystal growth.

Fig. 2 shows device resistance vs. write pulse width. The reset resistance saturates when the pulse width is long enough to achieve melting of the phase-change material. The set pulse adequately crystallizes the bit in 50 ns with a RESET/SET resistance ratio of greater than 100.

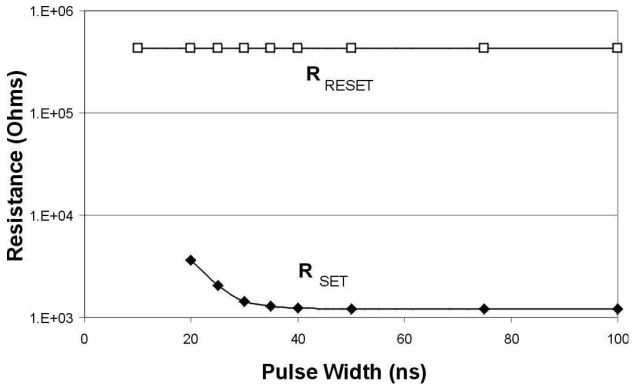

Fig. 2 Programmed resistance values of the SET and RESET states as a function of current pulse width.

Fig. 3 shows the I-V characteristics of the OUM device. At low voltage, the device exhibits either a low resistance (~1KΩ) or high resistance (>100KΩ), depending on its programmed state. This is the read region of operation. To program the device, a pulse of sufficient voltage is applied to drive the device into a high conduction "dynamic on state."

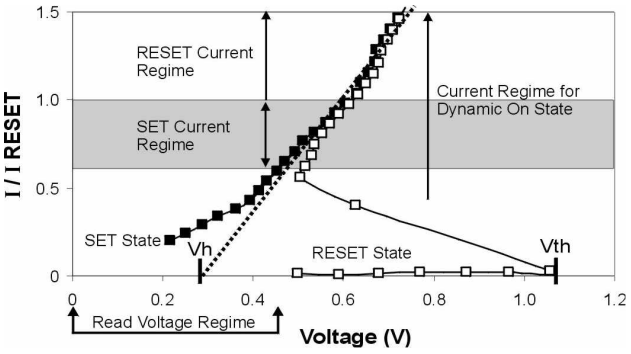

Fig. 3 I-V characteristics of memory element showing key device parameters: Read/SET/RESET regimes, SET and RESET states, Vh (Holding voltage) and Vth (Switching threshold voltage). The device current in the Read Voltage regime is substantial when reading the SET state but is insignificant for a reset device, allowing a large dynamic range and sense margin.

For a reset device, this requires a voltage greater than Vth. Vth is a device design parameter and for current memory applications is chosen to be in the range of 0.5-0.9V. To avoid read disturb, the device read region, as shown in the figure, is well below Vth and also below the reset regime. The device is programmed while it is in the dynamic on state. The final programmed state of the device is determined by the current amplitude and the pulse duration in the dynamic on state. The reciprocal slope of the I-V curve in the dynamic on state is the series device resistance.

Fig. 4 shows the device read resistance resulting from application of the programming current pulse amplitude. Starting in the set condition, moving from left to right, the device continues to remain in SET state as the amplitude is increased. Further increase in the pulse amplitude begins to reset the device with still further increase resetting the device to a saturated amorphous resistance. Beginning again with a device initially in the RESET state, low amplitude pulses at voltages less than Vth do not set the device. Once Vth is surpassed, the device switches to the dynamic on state and programmed resistance is dramatically reduced as crystallization of the material is achieved. Further increase in programming current further crystallizes the material, which drops the resistance to a minimum value. As the programming pulse amplitude is increased further, resetting again is exhibited as in the case above. Devices can be safely reset above the saturation point for margin. Importantly, the right side of the curve exhibits direct overwrite capability, where a particular resistance value can be obtained from a programming pulse, irrespective of the prior state of the material. The slope of the right side of the curve is a device design parameter and can be adjusted to enable a multi-state memory cell.

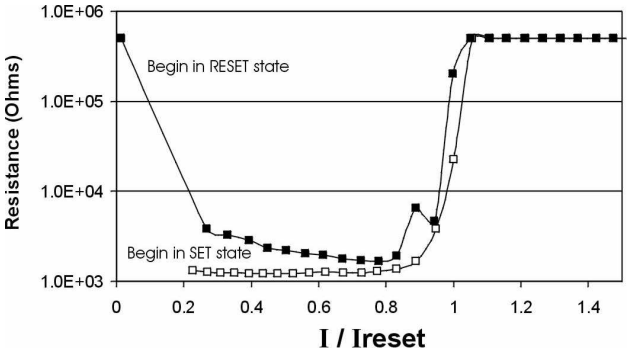

Fig. 4 R-I, or Resistance-Current pulse height characteristics of a memory element showing the change in resistance that results from different amplitude current pulses for both an initially set and a reset bit.

Device endurance has been demonstrated beyond 1E12 set/reset cycles. An example is shown in Fig. 5 with 30 ns reset and 50 ns set pulses. A RESET/SET resistance ratio > 60 was observed over the entire range. Cycling out to 1E13 set/reset cycles has been evaluated on some devices. Failure mechanisms at this level of cycling have been identified, and efforts are underway to extend the endurance.

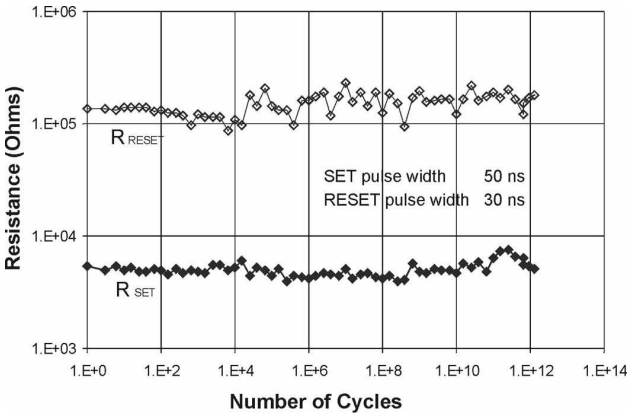

Fig.5 Cycling performance of the SET and RESET state of the memory element. No degradation in dynamic range was observed up to 1.25E12 cycles, and cycling was stopped.

Intrinsic data retention time as a function of ambient temperature under continuous read operation is shown in Fig. 6 as an Ahrrenius plot. Extrapolation to 10 year retention time at 120C is indicated.

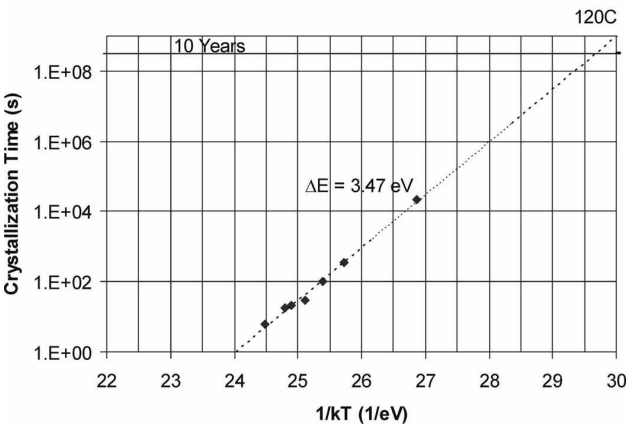

Fig. 6 Temperature induced time to set a RESET bit vs.1/kT.

SCALING

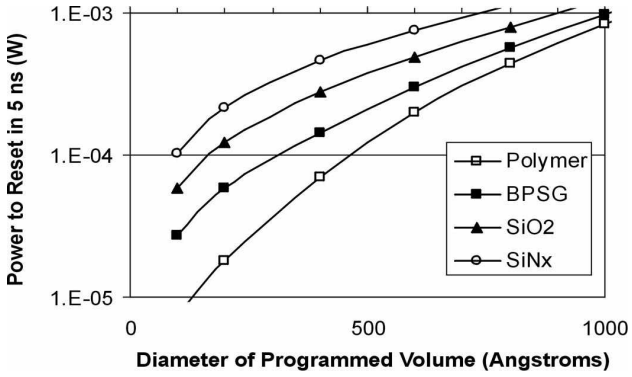

Fig. 7 Simulation results for a spherical programmed volume surrounded by different dielectric materials and scaling the diameter from 1,000 to 100 Angstroms. Scaling results in lower power and faster memory operation.

Fig. 7 shows computer simulation results of programming power vs. media volume for a simple spherical cell geometry, parameterized by the choice of dielectric material surrounding the cell element. Thermal isolation and reduction in the volume of programmed material are the key requirements to make a high density, low power memory.

CONCLUSIONS

Nonvolatile OUM with fast read and write speeds, high endurance, low voltage/low energy operation, ease of integration, and competitive cost structure is suitable for ultra-high density, stand alone and embedded memory applications. These attributes make OUM an attractive alternative to Flash memory technology and potentially competitive with volatile memory technologies.

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